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09/883,836	06/17/2001	Brian Bailey	51005.P220	9966

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EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 06/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/883,836	BAILEY ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 24-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 24-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 and 24-36 were examined.

Section I: Non-Final Office Action (3rd Office Action)

Claim Interpretation

2. Office personnel are to give claims their **"broadest reasonable interpretation"** in light of the supporting disclosure. *In re Morris,* 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater,* 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551(CCPA 1969). See *also *In re Zletz,* 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322(Fed. Cir. 1989) ("During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow") .... The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed .... An essential purpose of patent examination is to fashion claims that are precise, clear, correct, and unambiguous. Only in this way can uncertainties of claim scope be removed, as much as possible, during the administrative process. The examiner interprets "coherent" a using the results of a previous computation for re-calculation (Ravichandran: abstract, lines 14-15).

Claim Rejections - 35 USC § 103

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madden et al., (US Patent 5,119,483 (1992)) (hereafter Madden) in view of Peterson et al., (US Patent 6,983,237 (2006)) (hereafter Peterson) and in further view of Ravichandran (US Patent 5,966,537 (1999)). Madden, Peterson and Ravichandran are analogous arts since each one teaches electronic devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the plurality of simulations of Peterson; and selective instructions of the simulation of Ravichandran in the first and second state information of Madden because Peterson teaches a method that allows a modeler to view one or more parameters that are linked either in a predefined-manner for automatic linkage or that are linked manually by a modeler who copies experimental results for a preceding experiment for utilization (Peterson: column 4, line 61-64). Ravichandran teaches a dynamic optimizing compiler, which uses input data to profile a computer application in systematic manner suitable for producing a highly optimized executable (Ravichandran: column 2, lines 30-34).

Claim 1. A method comprising: identifying state information (Madden: column 18, lines 24-25) comprising a transfer from a first simulation model (Peterson: column 10, lines 33-44) in a simulation environment, said transfer being directed to a second simulation model (Peterson: column 10, lines 33-44) in a circuit design being simulation in the simulation environment; receiving the state information (Madden: column 18, lines

24-25) from the first simulation model; and making the state information available to the second simulation model (Peterson: column 10, lines 33-44) without simulating the transfer (Ravichandran: column 6, lines 39-41 "the simulation instructions will not be executed...") in the circuit design.

Claim 2. The method of claim 1 wherein simulating the transfer form the first simulation model (Peterson: column 10, lines 33-44) to the second simulation model (Peterson: column 10, lines 33-44) in the design comprises transferring the state information through at least one additional simulation model in the simulation environment.

Claim 3. The method of claim 1 wherein receiving the state information (Madden: column 18, lines 24-25) and making the state information available comprises: storing the state information in a coherent state memory space that is part of the simulation environment and corresponds to an element in the circuit design being simulated, said coherent state (see claim interpretation) memory space being accessible to both the first simulation model (Peterson: column 10, lines 33-44) and the second simulation model.

Claim 4. The method of claim 3 wherein the coherent state (see claim interpretation) memory space is accessible to a plurality of additional simulation (Peterson: column 9, lines 8-10) models.

Claim 5. The method of claim 1 wherein receiving the state information (Madden: column 18, lines 24-25) and making the state information available comprises at least one of a virtual transfer path for use when a simulation model of a transfer path in the circuit design is not included in the simulation environment (Ravichandran: transfer between original vectors and optimization vectors which appears separate from simulation event: column 8, lines 25-27); and a higher performance transfer path than the simulation model of the transfer path in the circuit design (path continues if changes pass optimization metric, if smaller, the optimization is completed, if not, more interactions continue Ravichandran: column 8, lines 8-24).

Claim 7. The method of claim 3 wherein the simulation environment comprises a plurality of additional simulation models, each of the plurality of additional simulation models (Duplication of Parts, MPEP 2144.04) corresponding to one or more of a plurality of additional coherent state (see claim interpretation) memory spaces, (Ravichandran: column 4, lines 40-42) the method further comprising: identifying additional state information comprising additional transfers among the plurality of additional simulation models (Duplication of Parts, MPEP 2144.04) in the simulation environment; and storing the additional state information (Ravichandran: stores state table: columns: 6, lines 60-65) in appropriate ones of the plurality of additional coherent state (see claim interpretation) state memory spaces such that the additional state information is accessible to corresponding of the plurality of additional simulation

models without simulating the additional transfer in the circuit design (Duplication of Parts, MPEP 2144.04).

6. Claims 6, 8-22, and 24-31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Madden, in view of Peterson and Ravichandran and further in view of Bailey et al., ("Hardware/Software Co-Simulation Strategies for the Future" (February 2000)). All four pieces of art are analogous because they teach electronic devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the embedded custom software/hardware simulation of ASIC/FPGA's of Bailey in the methods described in Madden, Peterson and Ravichandran because Bailey teaches an improved test and integration phase to improve the risk levels associated with on-time delivery (Bailey: pg. 3, 6th paragraph, lines 1-2).

Claim 6. The method of claim 5 (Ravichandran: column 5, lines 45-55) wherein the higher performance transfer path (Bailey: pg. 6, Accuracy paragraph, lines 7-9) provides a lower level of resolution (Bailey: pg. 6, cycle section, lines 1-3) than the simulation model of the transfer path in the circuit design.

Claim 8. The method of claim 1 (Ravichandran: column 5, lines 45-55) wherein the simulation environment comprises a plurality of simulation domains, (Duplication of Parts, MPEP 2144.04) the method comprising: selectively activating and deactivating

(selectively suppressing activity; Bailey: pg. 7, Cross-Domain Optimization section, lines 3-4) particular simulation domains in the simulation environment such that a resolution (Bailey: pg. 6, cycle section, lines 1-3) and a performance for the circuit design being simulated is dynamically modified (Ravichandran: column 2, lines 30-33) as the state information is received and made available.

Claim 9. The method of claim1 wherein the plurality of simulation domains (Duplication of Parts, MPEP 2144.04) comprise at least one of a software execution domain, (Ravichandran: column 1, lines 29-30) a hardware (Ravichandran: column 1, lines 43; column 2, lines 41-42) simulation domain, and an abstract (suggestion of a level of abstraction; Bailey: pg.4, Bus Functional Model, lines 7-8) model simulation domain.

Claim 10. The method of claim 9 wherein the software execution domain comprises at least one of a native processor package, an instruction set simulator (ISS), (suggestion of a level of an instruction set; Bailey: pg.4, Bus Functional Model, lines 7-8) and a programming language simulator to model software execution in one or more processors (mention of software execution; Bailey: pg. 3, 3rd paragraph, lines 4-6).

Claim 11. The method of claim 9 wherein the hardware simulation domain comprises at least one of a logic (Ravichandran: column 1, lines 43; column 2, lines 41-42) simulator and a programming language (Ravichandran: column 4, line 4) simulator.

Claim 12. The method of claim 11 wherein the logic simulator comprises one of a hardware description language (HDL) (Ravichandran: "C" and "C++" are examples of gate-level programming languages: column 4, lines 2-4) based simulator, a gate-level simulator (Bailey: pg. 6, Performance section, lines 4-7), a simulation accelerator (Bailey: pg. 6, Performance section, lines 6-7), a system simulator, a cycle simulator (Bailey: pg. 6, Cycle section), and a programmable hardware emulator (Bailey: pg. 6, Emulation section).

Claim 13. The method of claim 11 wherein the programming language (Bailey: pg. 4, Bus Function Model section, lines 1-3) simulator comprises at least one of a C programming language simulator, a C++ programming language simulator, (Ravichandran: column 4, lines 2-4) a simulator using a C-based language, a simulator using a C++ based language, and a JAVA (Ravichandran: column 1, lines 29-30) programming language simulator.

Claim 14. The method of claim 9 wherein the hardware simulation domain (Bailey: pg. 1, abstract, lines 7-9) comprises at least one simulation model of a circuit element in the circuit design (Ravichandran: e.g., microprocessors: column 10, lines 20-23).

Claim 15. The method of claim 8 further comprising: partitioning the circuit design (Bailey: pg. 2, 4th paragraph, lines 6-7) into the plurality of simulation domains

(Duplication of Parts, MPEP 2144.04) based on a partition criteria (Bailey: pg. 2, 4th paragraph, lines 6-7).

Claim 16. The method of claim 15 wherein the partition criteria (Bailey: pg. 2, 4th paragraph, lines 6-7) comprises at least one of an abstraction level, (suggestion of a level of abstraction; Bailey: pg.4, Bus Functional Model, lines 7-8) a simulation type, and a function type (suggestion of function type; Bailey: pg. 7, 4th paragraph).

Claim 17. The method of claim 16 wherein partitioning the circuit design based on the abstraction level (suggestion of a level of abstraction; Bailey: pg.4, Bus Functional Model, lines 7-8) partition the circuit deign into at least one of a pin-level domain (Bailey: pg. 5, Instruction Set Simulation section, lines 1-2), a bus-level domain (suggestion of function type; Bailey: pg. 7, 4th paragraph), and a transaction-level domain.

Claim 18. The method of claim 16 wherein partitioning (Bailey: pg. 2, 4th paragraph, lines 6-7) the circuit design based on the simulation type partitions the circuit design into at least one of a software execution domain (Bailey: pg. 4, paragraphs 4-7), a logic simulator domain, and a programming language (Ravichandran: column 4, line 4) simulator domain.

Claim 19. The method of claim 16 wherein partitioning the circuit design based on the function type comprises (suggestion of function type; Bailey: pg. 7, 4th paragraph):

identifying one or more function elements in the circuit design that have a particular level (example of a high-level; Bailey: pg. 5, lines3-5) of independent operation from the remainder of the circuit design; and defining of a domain (suggestion of domains; Bailey: pg.7, 4th paragraph) encompassing each identified functional element.

Claim 20. The method of claim 8 wherein each of the plurality of simulation domains (Duplication of Parts, MPEP 2144.04) provides a particular performance level and a particular resolution level, and wherein the particular simulation domains are selectively activated or deactivated (selectively suppressing activity; Bailey: pg. 7, Cross-Domain Optimization section, lines 3-4) during particular stages of simulation in combinations that either accelerate performance (Bailey: pg. 6, Performance section, lines 5-7) of the simulation environment or increase resolution of the simulation environment.

Claim 21. The method of claim 8 wherein selectively activating and deactivating (selectively suppressing activity; Bailey: pg. 7, Cross-Domain Optimization section, lines 3-4) the particular simulation domains (Inherent to any software simulation program: turning the simulation on or off) comprises (Duplication of Parts, MPEP 2144.04): identifying a system state of the circuit design; determining which of the plurality of simulation domains are to be active for the identifying system state; and advancing simulation time only in each activated simulation domain (Ravichandran: suggestion of discriminating instructions: column 6, lines 39-41).

Claim 22. The method of claim 21 wherein determining which of the plurality of simulation domains (simulation domains; Bailey: pg. 1, Abstract, lines 8-9 and figure 1| however, Duplication of Parts, MPEP 2144.04) are to be active for the identified system state comprises at least one of a centralized control, a transaction-based control, and a distributed control.

Claim 24. The method of claim 22 (simulation domains; Bailey: pg. 1, Abstract, lines 8-9 and figure 1| however, Duplication of Parts, MPEP 2144.04) wherein the system state comprises system addresses in the circuit design.

Claim 25. The method of claim 22 wherein the system state comprises a data transaction (Bailey: pg. 6, cycle section, lines 3-4) in the circuit design, said data transaction (Bailey: pg. 6, cycle section, lines 3-4) being configured with information identifying which of the plurality of simulation domains (Duplication of Parts, MPEP 2144.04) are to be active for the data transaction (Bailey: pg. 6, cycle section, lines 3-4), and wherein the transaction-based control comprises: sending a message to a centralized simulation clock as part of the data transaction (Bailey: pg. 6, cycle section, lines 3-4), said message to instruct the centralized simulation clock with respect to which of the plurality of simulation domains are to be active for the data transaction (Bailey: pg. 6, cycle section, lines 3-4).

Claim 26. The method of claim 22 (simulation domains; Bailey: pg. 1, Abstract, lines 8-9 and figure 1| however, Duplication of Parts, MPEP 2144.04) wherein a predetermined simulation domain is configured with activation information identifying at least one particular system state for which the predetermined simulation domain is to be active (section teaches whether to reduce or eliminate all further occurrences; Bailey: pg. 6, Accuracy Section, lines 6-9), wherein identifying the system state comprises receiving a broadcast of the system state at the predetermined simulation domain comprises determining if the predetermined simulation domain is to be active for the identifying system state based on the activation information (cycle state discloses scheduling timing details, i.e., current state of inputs; Bailey: pg. 6, 2nd paragraph); and advancing an operation in the predetermined simulation domain according.

Claim 27. The method of claim 26 wherein the information further identifies an event for terminating operation (Bailey: pg. 7, Cross-Domain Optimization section, lines 3-5) of the predetermined simulation domain for the at least one particular system state.

Clam 28. The method of claim 21 wherein determining which of the plurality of simulation domains (Duplication of Parts, MPEP 2144.04) are to be active for the identified system state depends on a plurality of control mechanisms (Duplication of Parts, MPEP 2144.04), wherein each of the plurality of control mechanisms comprises a priority level, and wherein a higher priority control mechanism takes precedence over a

lower priority control mechanism (section discusses importance of higher performance levels, thus describing priority; Bailey: Accuracy Section, lines 3-9).

Claim 29. The method of claim 8, wherein the plurality of simulation domains (Duplication of Parts, MPEP 2144.04) comprises a hierarchical structure and wherein selectively activating and deactivating (selectively suppressing activity; Bailey: pg. 7, Cross-Domain Optimization section, lines 3-4) the particular simulation domains is based on levels of the hierarchical structure.

Claim 30. The method of claim 1 wherein both the first simulation model (Peterson: column 10, lines 33-44) and the second simulation model (Peterson: column 10, lines 33-44) are within a same simulation domain in the simulation environment.

Claim 31. The method of claim 1, wherein the first simulation model (Peterson: column 10, lines 33-44) and the second simulation model (Peterson: column 10, lines 33-44)are within different simulation domains (inherent: first simulation (Ravichandran: column 7, line 65)is different from the second simulation) in the simulation environment.

7. Claims 32-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madden (US Patent 5,119,483 (1992)) in view of Peterson (US Patent 6,983,237 (2006)) and in further view of Bailey. Madden, Peterson and Bailey are analogous art since they all teach computer processors.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the plurality of simulations of Peterson and the embedded custom software/hardware simulation of ASIC/FPGA's of Bailey in the first and second state information of Madden because Peterson teaches a method that allows a modeler to view one or more parameters that are linked either in a predefined-manner for automatic linkage or that are linked manually by a modeler who copies experimental results for a preceding experiment for utilization (Peterson: column 4, line 61-64). Bailey teaches an improved test and integration phase to improve the risk levels associated with on-time delivery (Bailey: pg. 3, 6th paragraph, lines 1-2).

Claim 32. The method comprising: reading state information from a first simulation model (Peterson: column 10, lines 33-44) in a simulation environment when a simulation domain of the first simulation model (Peterson: column 10, lines 33-44)is deactivated (selectively suppressing activity; Bailey: pg. 7, Cross-Domain Optimization section, lines 3-4); and writing the state information to a second simulation model (Peterson: column 10, lines 33-44) in the simulation environment prior to activation of a simulation domain of the second simulation model, said first simulation model (Peterson: column 10, lines 33-44)and said second simulation model (Peterson: column 10, lines 33-44) representing different version of a same functionality in a circuit design being simulation.

Claim 33. The method of claim 32 wherein the first simulation model (Peterson: column 10, lines 33-44)and the second simulation model (Peterson: column 10, lines 33-44)each have a particular level of performance and resolution, and wherein simulation of the circuit design switches from the first simulation model (Peterson: column 10, lines 33-44)to the second simulation model (Peterson: column 10, lines 33-44) is based on a change in a performance level and/or a resolution level desired at a difference stage of simulation.

Claim 34. The method of claim 32 wherein the first simulation model (Peterson: column 10, lines 33-44) and the second simulation model (Peterson: column 10, lines 33-44) are among a plurality of simulation models (Duplication of Parts, MPEP 2144.04) representing a same functionality in the circuit design, each of the plurality of simulation models (simulation domains; Bailey: pg. 1, Abstract, lines 8-9 and figure 1| however, Duplication of Parts, MPEP 2144.04) having a particular level of performance and resolution, and each of the plurality of simulation models (Duplication of Parts, MPEP 2144.04) being used at different stages of simulation depending on a desired performance level and/or resolution level of the simulation.

Claim 35. A machine readable medium having stored thereon machine executable instructions (Bailey: pg. 5, Instruction Set Simulation, 1st paragraph) that when executed implement a method comprising: identifying state information comprising a transfer from a first simulation model (Peterson: column 10, lines 33-44) in a simulation

environment, said transfer being directed to a second simulation model (Peterson: column 10, lines 33-44) in a circuit design being simulation environment; receiving the state information (Madden: column 18, lines 24-25) from the first simulation model; and making the state information available to the second simulation model (Peterson: column 10, lines 33-44) without simulating the transfer in the circuit.

Clam 36. A machine readable medium having stored thereon machine executable instructions (Bailey: pg. 5, Instruction Set Simulation, 1st paragraph) that when executed implement a method comprising: reading state information from a first simulation model (Peterson: column 10, lines 33-44) in a simulation environment when a simulation domain of the first simulation model (Peterson: column 10, lines 33-44) is deactivated (selectively suppressing activity; Bailey: pg. 7, Cross-Domain Optimization section, lines 3-4); and writing the state information to a second simulation model (Peterson: column 10, lines 33-44) in the simulation environment prior to activation of a simulation domain of the second simulation model, said first simulation model (Peterson: column 10, lines 33-44) and said second simulation model (Peterson: column 10, lines 33-44) representing different versions (design choice) of a same functionality in a circuit design being simulated.

Section II: Response to Applicants' Arguments (Previous Office Action)

Objection to Specification

8. Box denoting objection to the specification in the office action summary was mistakenly checked. Objection is withdrawn.

102(b) and 103(a)

9. Applicant's arguments, see pages 11-16, filed 20 March 2006, with respect to the rejections of claims 1-5, and 7 under 35 U.S.C. 102(b) and 6,8-22 and 24-36 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Madden, Peterson, Ravichandran, and Bailey.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Paul Rodriguez 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

May 29, 2006

TS

Paul L. Rodriguez 9/6/06

Primary Examiner
Art Unit 2125